# 40A DrMOS Power Module with Integrated Diode Emulation and Thermal Warning Output

## ISL99140

The ISL99140 is a high performance DrMOS power module designed for high frequency power conversion. By combining a high performance FET driver and MOSFETS in an advanced package, high density DC/DC converters may be created. Combined with an Intersil PWM controller, a complete voltage regulator solution can be created with reduced external components and minimum overall PCB real estate.

The ISL99140 features a three-state PWM input that, working together with Intersil's multiphase PWM controllers, will provide a robust solution in the event of abnormal operating conditions. To further support robust applications, the ISL99140 features a thermal warning output that may be used to notify the power system of an impending thermal fail event.

The ISL99140 supports high efficiency operation not only at heavy loads, but also at light loads via its diode emulation capability. Diode emulation can be disabled for those applications where variable frequency operation is not desired at light loads.

## Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

## Features

- Compliant with Intel DrMOS Rev 4.0 specifications
- 40A average output current capability
- Supports 3-State 3.3V PWM input
- Supports 2-state 5V PWM input
- Thermal warning output
- Diode emulation option
- Adaptive shoot-through protection
- Integrated high-side gate-to-source resistor to prevent self turn-on due to high input bus dV/dt
- Undervoltage lockout
- Switching frequencies up to 2MHz
- Pb-Free (RoHS Compliant)
- 6x6 QFN package

## Applications

- High frequency and high efficiency VRM and VRD
- Core, graphic, and memory regulators for microprocessors
- High density VR for server, networking and cloud computing
- POL DC/DC converters and video gaming consoles

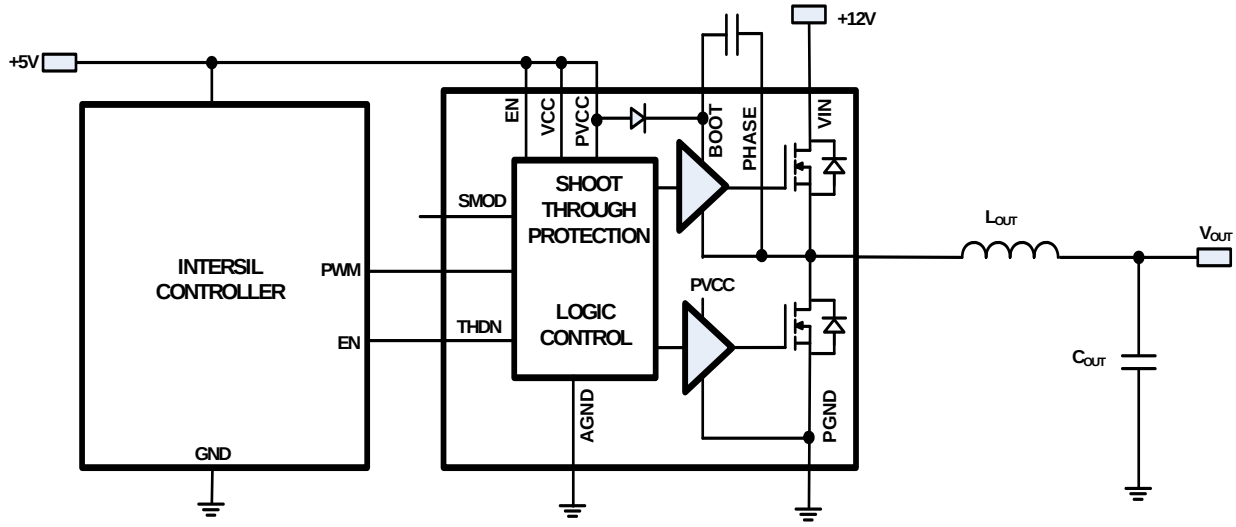



FIGURE 1. SIMPLIFIED APPLICATION BLOCK DIAGRAM

# Ordering Information

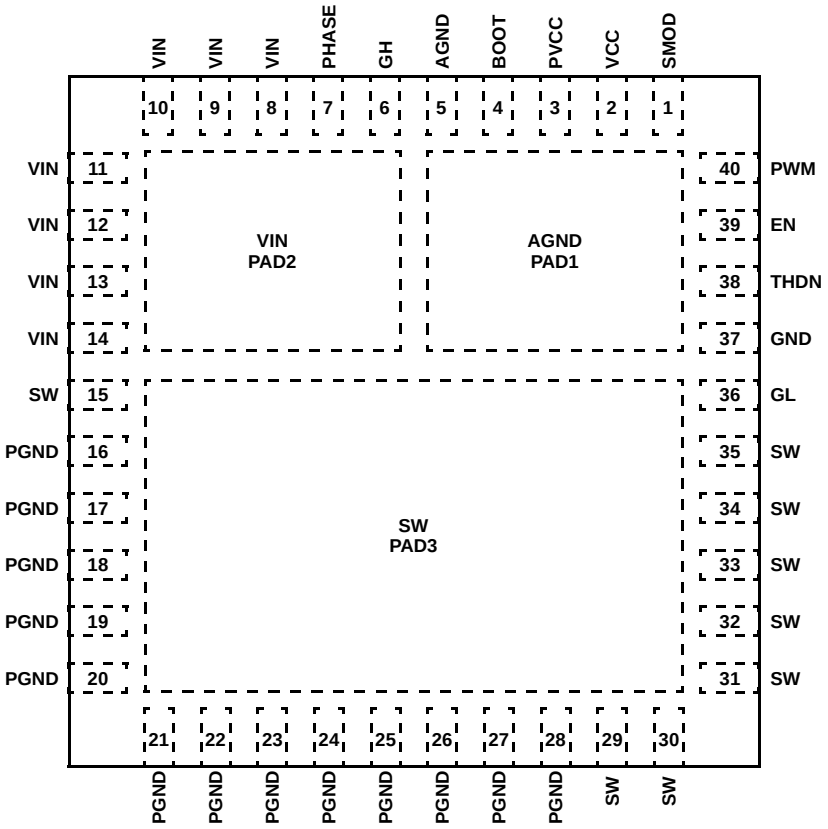
| PART NUMBER (Notes 1, 2, 3) | PART MARKING | TEMP RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|---|
| ISL99140IRZ | 99140 IRZ | -40 to +85 | 40 Ld Exposed Pad 6x6 QFN | L40.6X6A |

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL99140. For more information on MSL, please see tech brief TB363.

# Pin Configuration

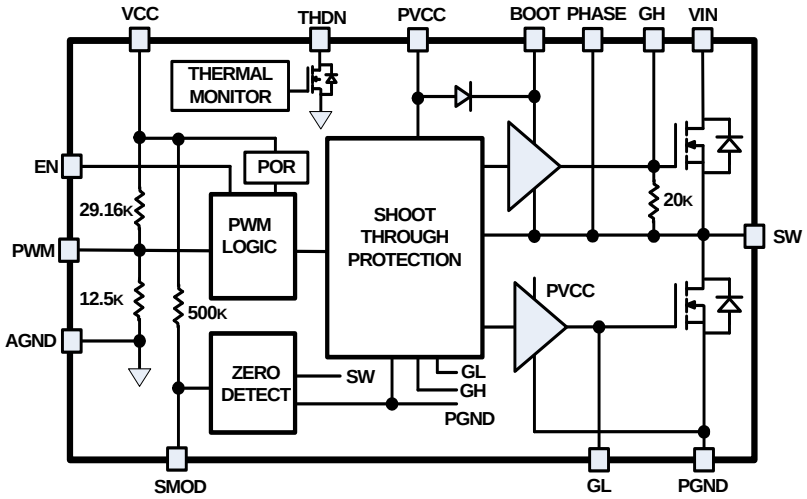
ISL99140
(40 LD QFN)
TOP VIEW



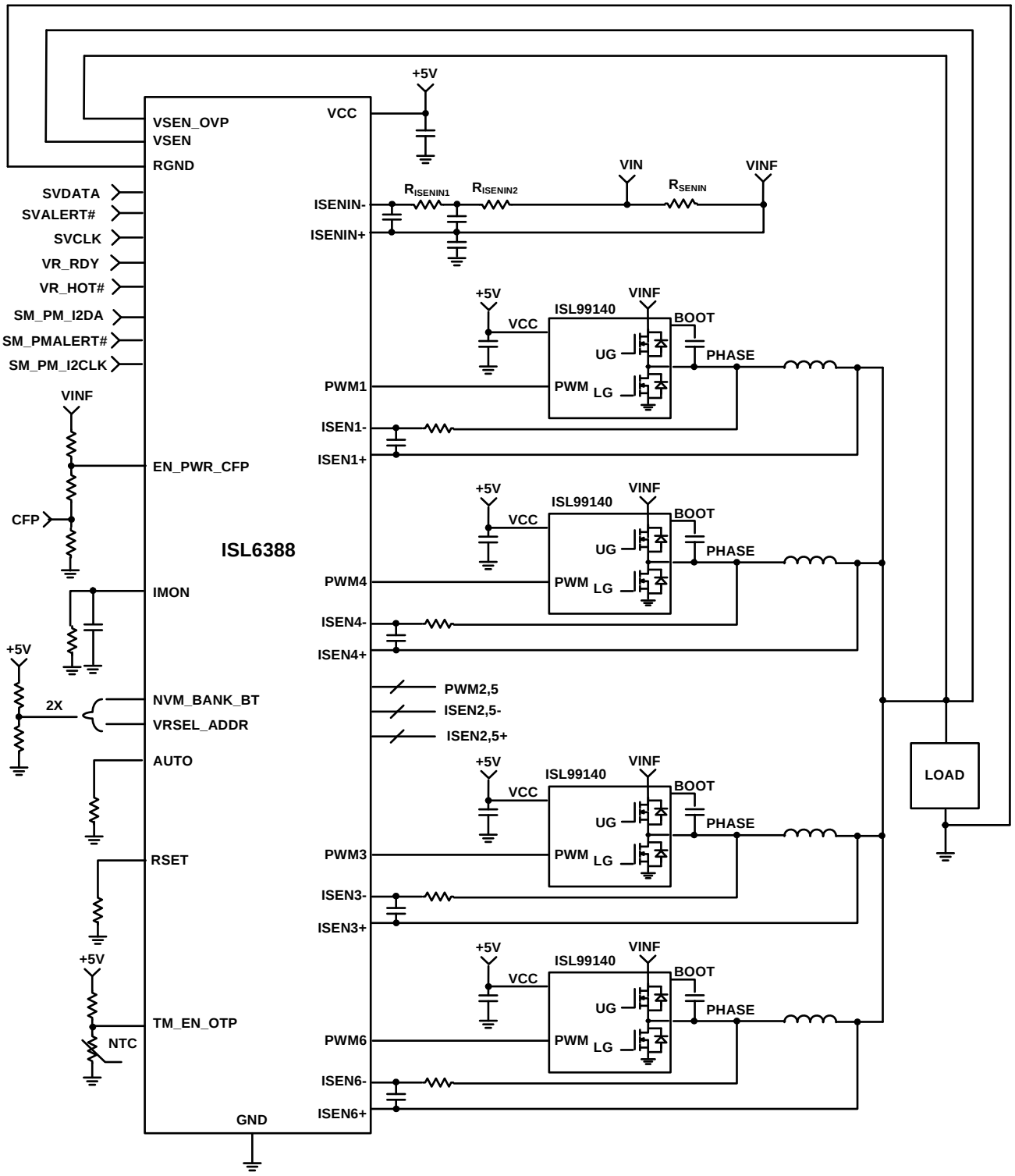
## Pin Descriptions

| PIN # | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | SMOD | Input pin to enable or disable Diode Emulation with built-in pull up of 10µA. When SMOD is LOW, diode emulation is allowed. Otherwise, continuous conduction mode is forced. |
| 2 | VCC | +5V logic bias supply. Place a high quality low ESR ceramic capacitor from this pin to GND. |
| 3 | PVCC | +5V driver bias supply. Place a high quality low ESR ceramic capacitor from this pin to GND. VCC and PVCC often share the decoupling capacitor (~1µF/0402~0603/ X5R~X7R). |
| 4 | BOOT | Floating bootstrap supply pin for the upper gate drive. Place a high quality low ESR ceramic capacitor (~0.1µF to 0.22µF) in close proximity across BOOT and PHASE pins. |
| 5, 37, PAD1 | AGND, GND | Return of logic bias supply VCC. Connect directly to system ground plane. |
| 6 | GH | High-side gate drive output for monitoring/testing. No circuit connection needed. |
| 7 | PHASE | Return of bootstrap capacitor. Internally connected to SW node. External connection is not needed. |
| 8, 9, 10, 11, 12, 13, 14, PAD2 | VIN | Input of Power Stage. Place couple high quality low ESR ceramic capacitor (couple 10µF or higher, X7R) in close proximity across VIN and GND planes. |
| 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28 | PGND | Power Stage return. Connect directly to system ground plane. |
| 15, 29, 30, 31, 32, 33, 34, 35, PAD3 | SW | Switching junction node between low and high-side MOSFETs. Connect directly to output inductor. |
| 36 | GL | Low-side gate drive output for monitoring/testing. No circuit connection needed. |
| 38 | THDN | Thermal warning flag, an output open drain pin. High = Normal operation; Low = Shutdown. |
| 39 | EN | Enable input pin with 2µA internal weak pull-down. High = Enable; Low = Disable. |
| 40 | PWM | PWM input of gate driver. The PWM signal can enter three distinct states during operation. Connect this pin to the PWM output of the controller. |

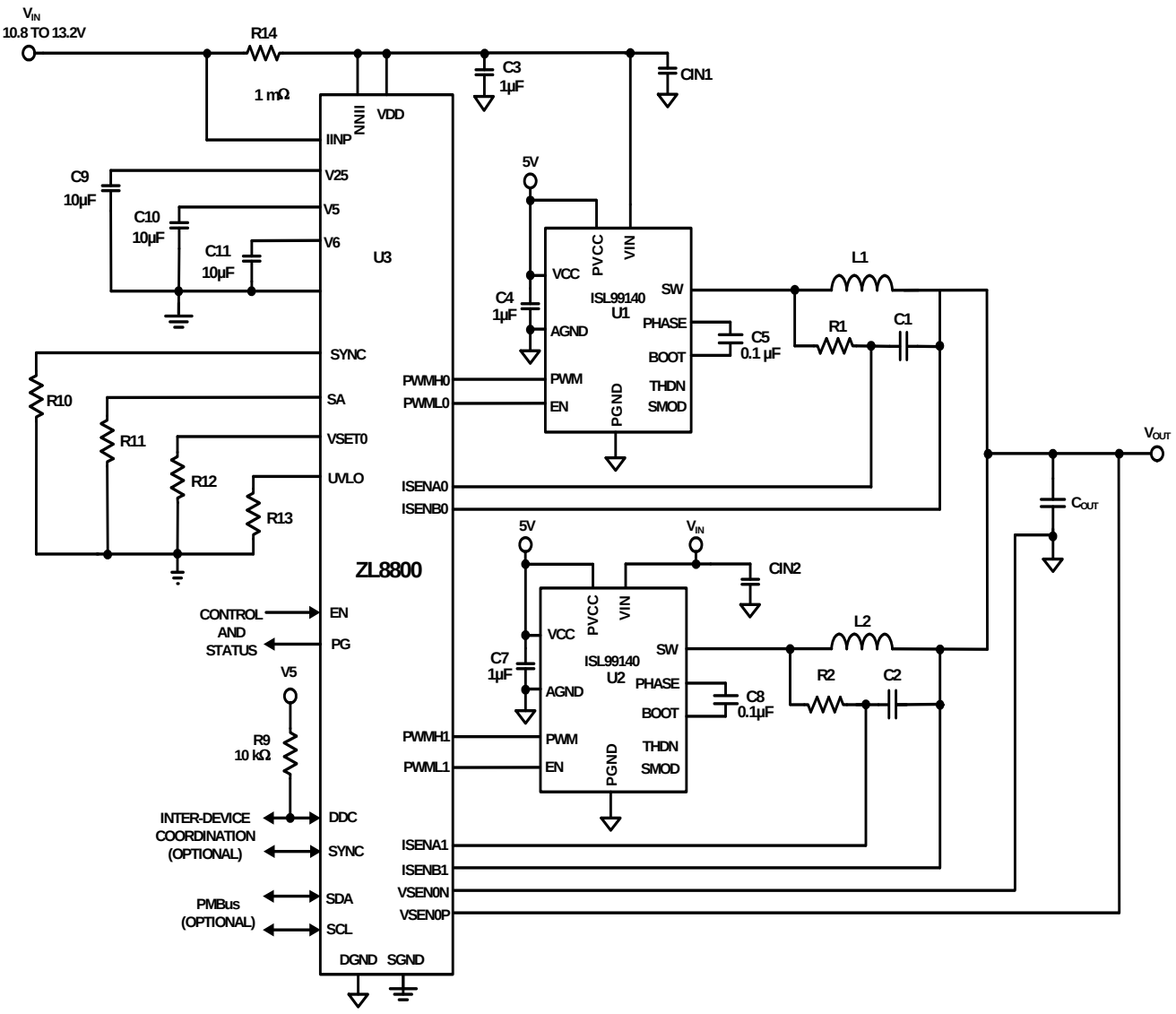
## Functional Block Diagram



## Typical Application Circuit with ISL6388



## Typical Application Circuit with ZL8800



## Absolute Maximum Ratings

VIN . . . . . -0.3V to 30V
Supply Voltage (VCC) . . . . . -0.3V to 7V
I/O Voltage ($V_{EN}$, $V_{PWM}$, $V_{SMOD}$, $V_{THDN}$) . . . . . -0.3V to VCC + 0.3V
BOOT Voltage ($V_{BOOT-GND}$) . . . . . -0.3V to 25V (DC) or 36V (<200ns)
BOOT To PHASE Voltage ($V_{BOOT-PHASE}$) . . . . . -0.3V to 7V (DC)
. . . . . -0.3V to 9V (<10ns)

## Thermal Information

| Thermal Resistance | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 40 Ld 6x6 QFN Package (Notes 4, 5) . . . . | 50 | 5 |

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

## Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to +85°C
Maximum Operating Junction Temperature . . . . . +125°C
Supply Voltage, VCC, PVCC . . . . . 5V ±5%
Input Supply Voltage, VIN . . . . . 4.5V to 18V

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

4. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.
6. Jedec Class II pulse conditions and failure criterion used.

## Electrical Specifications

$T_A$ = +25°C; $V_{IN}$ = 12V, $V_{VCC}$ = $V_{PVCC}$ = 5V Unless otherwise noted. **Boldface limits apply across the recommended operating temperature range.**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $V_{CC}$ Standby Supply Bias Current | $I_{VCC}$ | EN = Low, $V_{VCC}$ = 5V | | 187 | | µA |
| | | EN = High, $V_{PWM}$ = Open | | 467 | | µA |
| | | EN = High, $V_{PWM}$ = 0V | | 664 | | µA |
| PVCC Supply Bias Current | $I_{PVCC}$ | EN = High, $V_{PWM}$ = 300kHz, 50% Duty Cycle | | 23 | | mA |
| | | EN = High, $V_{PWM}$ = 1MHz, 50% Duty Cycle | | 51 | | mA |
| **POWER-ON RESET AND ENABLE** | | | | | | |
| POR Rising Threshold | $V_{PORR}$ | | | 3.40 | **3.9** | V |
| POR Falling Threshold | $V_{PORF}$ | | **2.3** | 2.92 | | V |
| POR Hysteresis | $V_{PORH}$ | | | 570 | | mV |
| EN High Threshold | $V_{ENH}$ | | **2.0** | | | V |
| EN Low Threshold | $V_{ENL}$ | | | | **0.8** | V |
| EN Pull Down Current | $I_{ENL}$ | | | 2 | | µA |
| **PWM INPUT** | | | | | | |
| Pull-Up Impedance | | | | 29.1 | | kΩ |
| Pull-Down Impedance | | | | 12.5 | | kΩ |
| PWM Rising Threshold | $V_{PWMH}$ | $V_{VCC}$ = 5V | **1.70** | 2.05 | **2.35** | V |
| PWM Falling Threshold | $V_{PWML}$ | $V_{VCC}$ = 5V | **0.75** | 1.00 | **1.25** | V |
| PWM Tri-State Rising Threshold | $V_{TRIH}$ | $V_{VCC}$ = 5V | **1.10** | 1.32 | **1.50** | V |
| PWM Tri-State Falling Threshold | $V_{TRIL}$ | $V_{VCC}$ = 5V | **1.60** | 1.75 | **1.95** | V |
| PWM Tri-State Rising Hysteresis | $V_{TRRH}$ | $V_{VCC}$ = 5V | | 310 | | mV |
| PWM Tri-State Falling Hysteresis | $V_{TRFH}$ | $V_{VCC}$ = 5V | | 310 | | mV |

**Electrical Specifications** $T_A$ = +25°C; $V_{IN}$ = 12V, $V_{VCC}$ = $V_{PVCC}$ = 5V Unless otherwise noted. **Boldface limits apply across the recommended operating temperature range. (Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| **SWITCHING TIME** | | | | | | |
| GH Turn-on Propagation Delay | $t_{PDHU}$ | $V_{VCC}$ = 5V, See Figure 2 (GL Low to GH High) | | 15 | | ns |
| GH Turn-off Propagation Delay | $t_{PDLU}$ | $V_{VCC}$ = 5V, See Figure 2 (PWM Low to GH Low) | | 18 | | ns |
| GL Turn-on Propagation Delay | $t_{PDHL}$ | $V_{VCC}$ = 5V, See Figure 2 (GH Low to GL High) | | 20 | | ns |
| GL Turn-off Propagation Delay | $t_{PDLL}$ | $V_{VCC}$ = 5V, See Figure 2 (PWM High to GL Low) | | 18 | | ns |
| GH/GL Exit Tri State Propagation Delay | $t_{PDTS}$ | $V_{VCC}$ = 5V, See Figure 2 (Tri-State to GH/GL High) | | 20 | | ns |
| Tri-State Shutdown Hold-off Time | $t_{TSSHD}$ | $V_{VCC}$ = 5V, See Figure 2 | **75** | 150 | **225** | ns |
| Minimum GL On-Time in DCM | $t_{LGMIN}$ | $V_{VCC}$ = 5V | | 350 | | ns |
| **SMOD INPUT** | | | | | | |
| SMOD High Threshold | $V_{SMODH}$ | | **2.0** | | | V |
| SMOD Low Threshold | VSMODL | | | | **0.8** | V |
| SMOD Pin Pull-up Current | ISMOD | | | 10 | | µA |
| **THERMAL SHUTDOWN (THDN)** | | | | | | |
| Pull-Down Impedance | | 1mA | | 60 | | Ω |
| Output Low | | 1mA | | 70 | | mV |
| Thermal Shutdown Flag Set | | (Note 8) | | 150 | | °C |
| Thermal Shutdown Flag Clear | | (Note 8) | | 135 | | °C |
| Hysteresis | | (Note 8) | | 15 | | °C |

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
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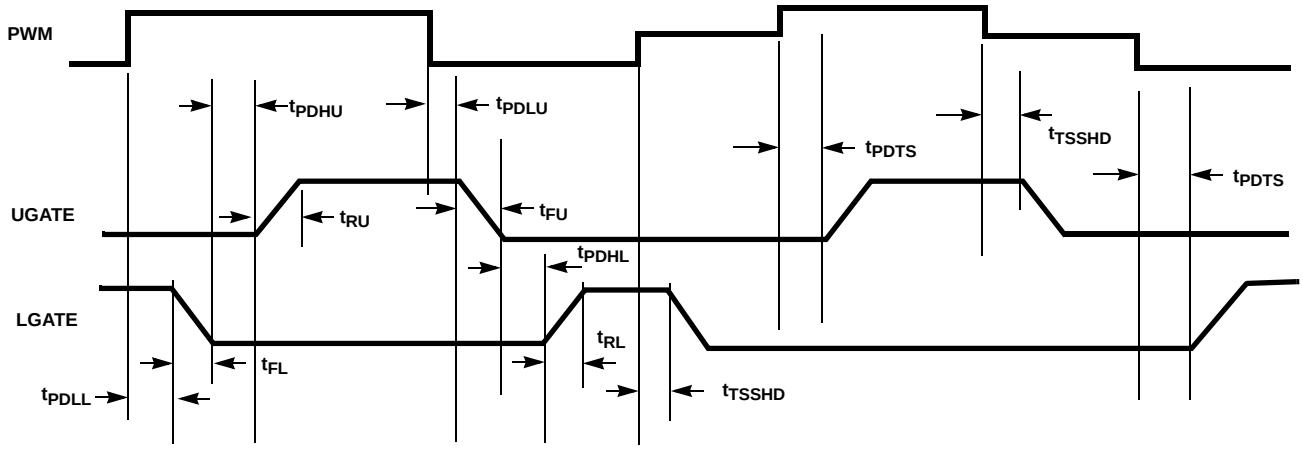



FIGURE 2. TIMING DIAGRAM

TABLE 1. GATE DRIVE TRUTH TABLE

| Enable | SMOD | PWM | GL | GH |
|---|---|---|---|---|
| L | X | X | L | L |
| H | L | L | H* | L |
| H | L | H | L | H |
| H | H | L | H | L |
| H | H | H | L | H |

NOTE: The LG stays high until inductor current drops to zero.

# Operation

The ISL99140 is an optimized driver and power stage solution for high density synchronous DC\DC power conversion. The ISL99140 includes a high performance driver, integrated Schottky bootstrap diode and MOSFET pair optimized for high switching frequency buck voltage regulators. The ISL99140 includes a driver with advanced power management features that allow direct control of the Lower MOSFET, Diode Emulation and thermal protection.

## Power-On Reset (POR) and EN

During initial start-up, the $V_{CC}$ voltage rise is monitored. Once the rising $V_{CC}$ voltage exceeds 3.5V (typically), normal operation of the driver is enabled. If $V_{CC}$ drops below the falling threshold of 2.95V (typically), operation of the driver is disabled.

Should the EN pin be pulled low, the driver will immediately force both MOSFETS to their off states. This action does not depend on the state of the PWM input.

## Shoot-through Protection

Prior to $V_{CC}$ exceeding its POR level, the undervoltage protection function is activated and both GH and GL are held active low (off). Once the $V_{CC}$ voltage surpasses the Rising Threshold (see “Electrical Specifications” on page 6) the PWM, SMOD and DE signals are used to control both high-side and low-side MOSFETs.

The rising edge on PWM initiates the turn-off of the lower MOSFET. Adaptive shoot-through circuitry monitors the GL voltage and determines a safe time for the upper MOSFET to turn-on. This prevents the MOSFET’s from conducting simultaneously.

The falling PWM transition causes the upper FET to turn-off and the lower FET to turn-on. Adaptive shoot-through circuitry monitors the GH to SW voltage to determine a safe time for low-side MOSFET turn-on. This prevents the MOSFET’s from conducting simultaneously.

Should the driver have no bias voltage applied and be unable to actively hold the MOSFETs off, an integrated 20kΩ resistor from the upper MOSFET gate-to-source will aid in keeping the device in its off state. This can be especially critical in applications where the input voltage rises prior to the ISL99140 $V_{CC}$ /PVCC supplies.

## Tri-State PWM Input

The ISL99140 supports a tri-level input on the PWM pin. Should the pin be pulled into and remain in the tri-state window for a set holdoff time, the driver will force both MOSFETs to their off states. When the PWM signal moves outside the shutdown window, the driver immediately resumes driving the MOSFETs according to the PWM commands.

This feature is utilized by Intersil PWM controllers as a method of forcing both MOSFETs off. Should the PWM input be left floating, the pin will be pulled into the tri-state window internally and force both MOSFETs to a safe off state. The ISL99140’s tri-state levels are compatible with 3.3V PWM logic.

Although PWM input can sustain as high as $V_{CC}$, the ISL99140 is not compatible with a controller (such as ISL637x family) that actively drives its mid level in tri-state higher than 1.7V. However,

the ISL99140 can be configured to be compatible with ZL8800 by connecting PWMH to PWM and PWML to EN, as shown in "Typical Application Circuit with ZL8800" on page 5. In this example, the tri-state operation is controlled by PWML output of ZL8800 through ISL99140's EN input. For detailed design information, consult the ZL8800 datasheet.

## Diode Emulation

Diode emulation allows for higher converter efficiency under light load situations. With diode emulation active (SMOD pulled low), the ISL99140 will detect the zero current crossing of the output inductor and turn off the Low-side gate after the minimum LGATE ON time of 350ns expires. This ensures that discontinuous conduction mode (DCM) is achieved to minimize losses. Diode emulation is asynchronous to the PWM signal. Therefore, the ISL99140 will respond to the SMOD input immediately after it changes state.

## Bootstrap Function

The ISL99140 features an internal bootstrap Schottky diode. A high quality ceramic capacitor should be place in close proximity across BOOT and PHASE pins. The bootstrap capacitor can range between 0.1µF~0.22µF/0402~0603/X5R~X7R for normal buck switching applications.

## Thermal Shutdown Warning (THDN)

The THDN pin is an open drain output and is pulled low when the internal junction temperature exceeds +150°C. The ISL99140 does not stop operation when the flag is set. This signal is often fed back to the controller to issue a system thermal shutdown. When the junction temperature drops below +135°C, the device will clear the THDN signal.

# PCB Layout Considerations

Proper PCB layout will reduce noise coupling to other circuits, improve thermal performance, and maximize the efficiency. The following is meant to lead to an optimized layout:

- Place multiple 10µF or greater ceramic capacitors directly at device between $V_{IN}$ and PGND as indicated in Figure 3. This is the most critical decoupling and reduced parasitic inductance in the power switching loop. This will reduce overall electrical stress on the device as well as reduce coupling to other circuits. Best practice is to place the decoupling capacitors on the same PCB side as the device.
- Connect PGND to the system GND plane with a large via array as close to the PGND pins as design rules allow. This improves thermal and electrical performance.
- Place PVCC, $V_{CC}$ and BOOT-PHASE decoupling capacitors at the IC pins as shown in Figure 3.
- Note that the SW plane connecting the ISL99140 and inductor must carry full load current and will create resistive loss if not sized properly. However, it is also a very noisy node that should not be oversized or routed close to any sensitive signals. Best practice is to place the inductor as close to the device as possible and thus minimizing the required area for the SW connection. If one must choose a long route of either the $V_{OUT}$ side of the inductor or the SW side, choose the quiet $V_{OUT}$ side. Best practice is to locate the ISL99140 as close to the final load as possible and thus avoid noisy or lossy routes to the load.

**TABLE 2. AVAILABLE EVALUATION BOARDS**

| EVALUATION BOARDS | DESCRIPTION | SMBus/ PMBus/$I^2C$ |
|---|---|---|
| ISL6388EVAL1Z | 6-Phase Core VR with ISL99140, 6x6 DrMOS, and the ISL6388, EAPP Digital Controller; Socket R3 | Yes |
| ISL6398EVAL1Z | 3-Phase POL VR with ISL99140, 6x6 DrMOS, and the ISL6388, EAPP Digital Controller; On-board Transient Load | Yes |

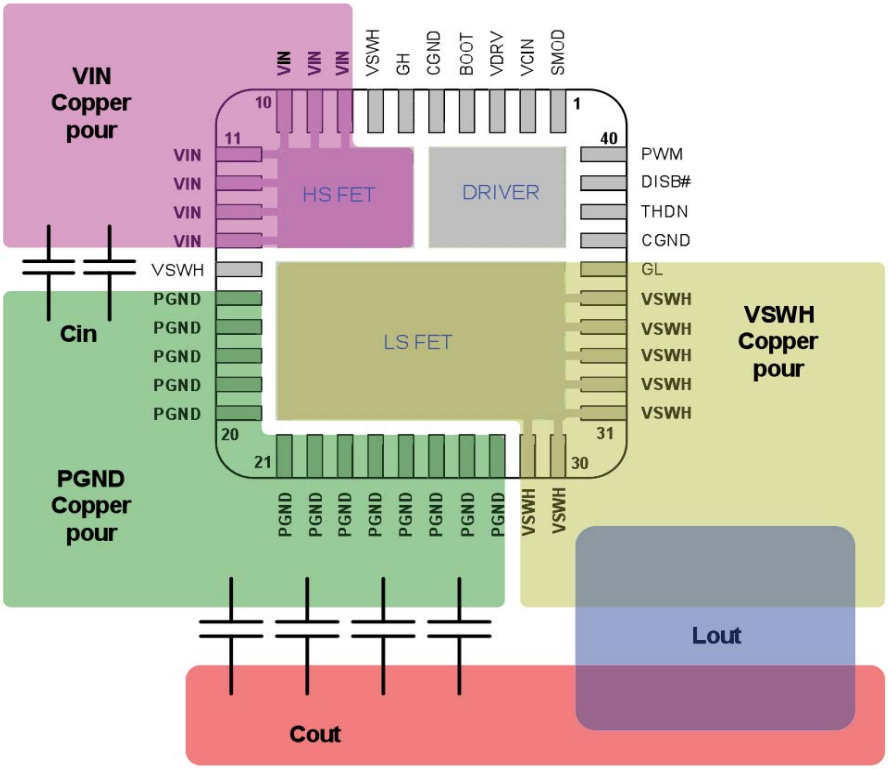



FIGURE 3. PCB LAYOUT FOR MINIMIZING CURRENT LOOPS

# Typical Performance Characteristics

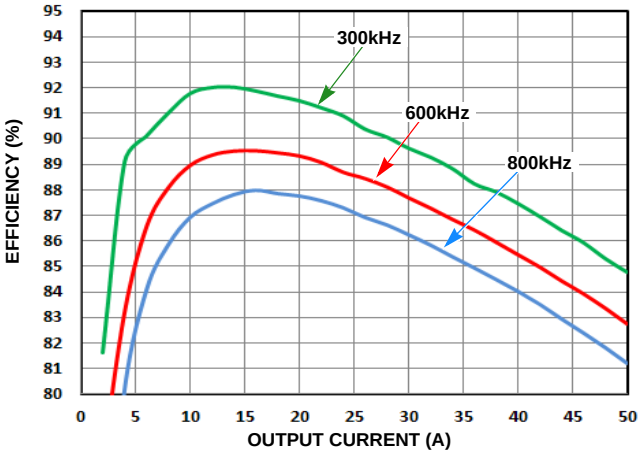



FIGURE 4. 1.0V $V_{OUT}$ POWER STAGE EFFICIENCY ($V_{IN}$ = 12V, $V_{CC}$ = $P_{VCC}$ =5V; $L_{OUT}$ = 0.23µH, 0.23mΩ, SLC1175-231; INCLUDE INDUCTOR AND ISL99140 LOSSES)

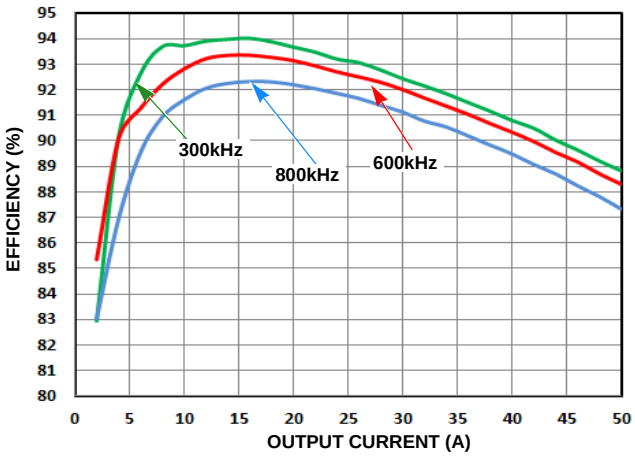



FIGURE 5. 1.8V $V_{OUT}$ POWER STAGE EFFICIENCY (VIN = 12V, $V_{CC}$ = $P_{VCC}$ = 5V; $L_{OUT}$ = 0.23µH, 0.23mΩ, SLC1175-231; INCLUDE INDUCTOR AND ISL99140 LOSSES)

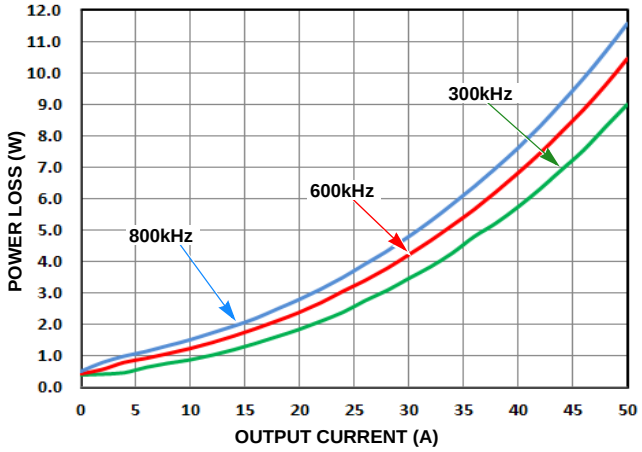



FIGURE 6. 1.0V $V_{OUT}$ POWER STAGE DISSIPATION ($V_{IN}$ = 12V, $V_{CC}$ = $P_{VCC}$ = 5V; $L_{OUT}$ = 0.23µH, 0.23mΩ, SLC1175-231; INCLUDE INDUCTOR AND ISL99140 LOSS)

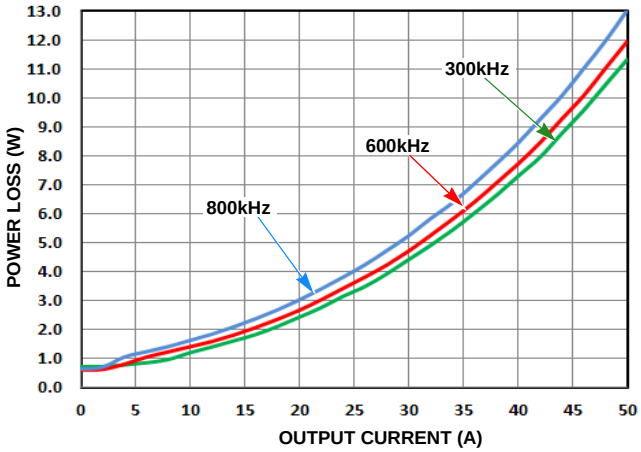



FIGURE 7. 1.8V $V_{OUT}$ POWER STAGE DISSIPATION ($V_{IN}$ = 12V, $V_{CC}$ = PVCC = 5V; $L_{OUT}$ = 0.23µH, 0.23mΩ, SLC1175-231; INCLUDE INDUCTOR AND ISL99140 LOSSES)

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| May 5, 2014 | FN8642.0 | Initial Release. |

# About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

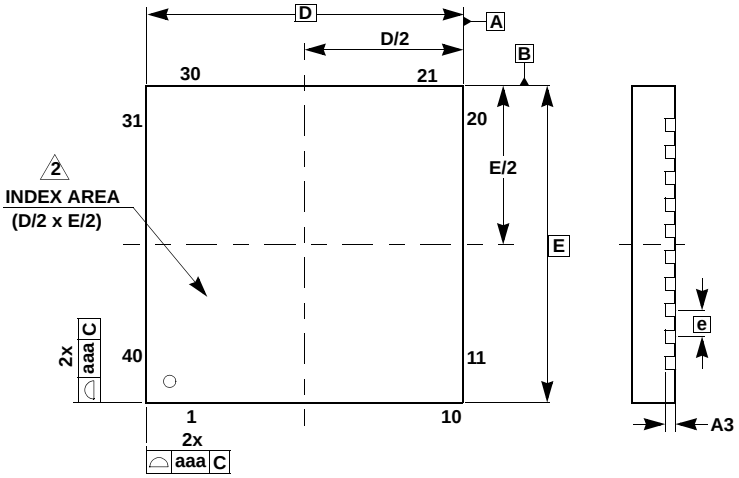
Reliability reports are also available from our website at www.intersil.com/support

# Package Outline Drawing

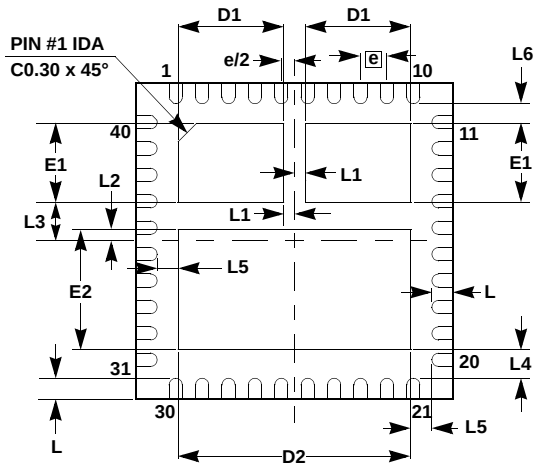
## L40.6x6A

**40 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE**

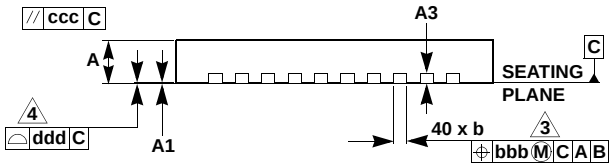
**Rev 0, 3/14**




TOP VIEW




BOTTOM VIEW



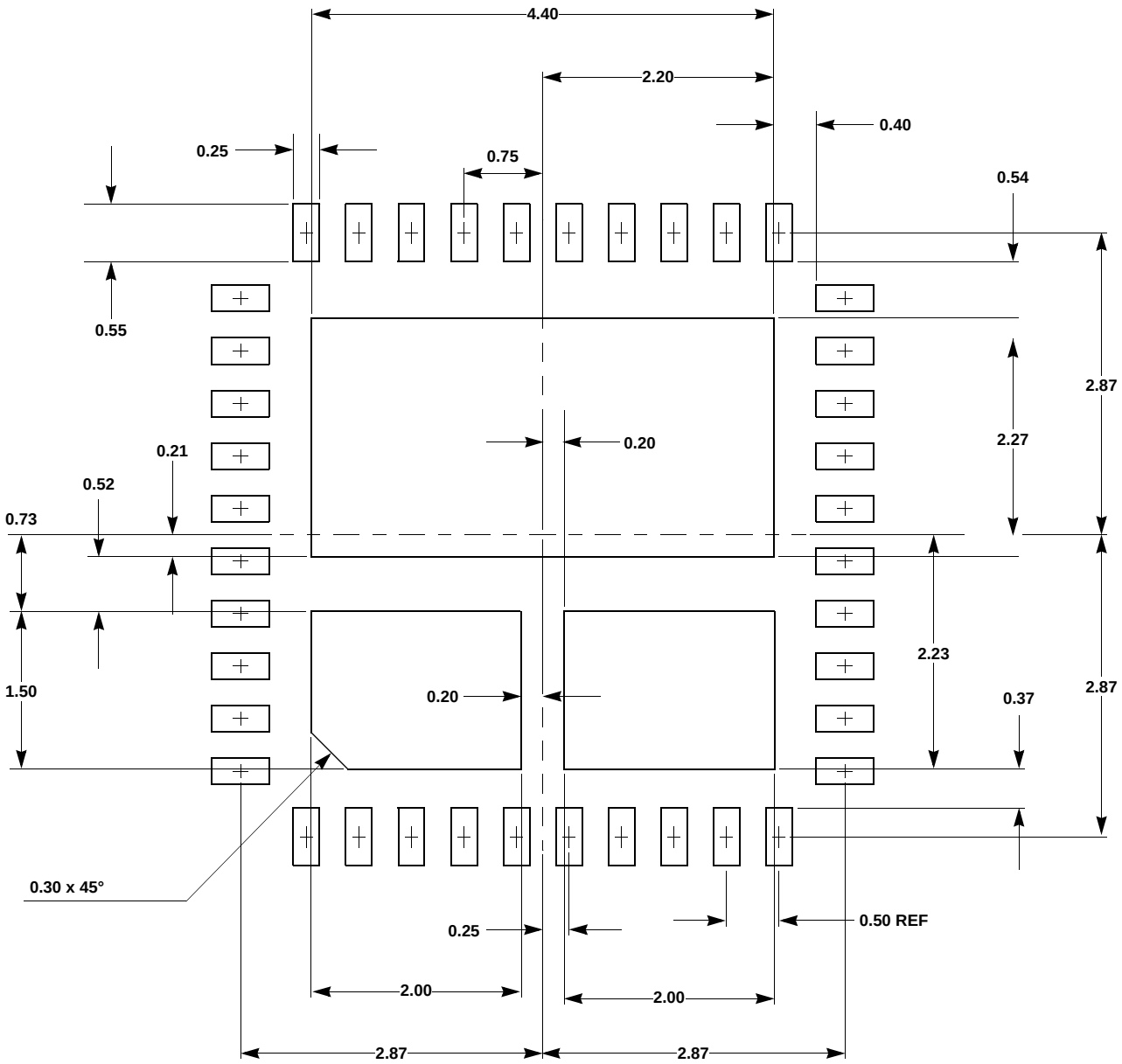

SIDE VIEW

**DIMENSIONS IN MILLIMETERS**

| SYMBOLS | MIN | TYP | MAX |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.20 | 0.25 | 0.35 |
| D | | 6.00 BSC | |
| D1 | 1.90 | 2.00 | 2.10 |
| D2 | 4.30 | 4.40 | 4.50 |
| E | | 6.00 BSC | |
| E1 | 1.40 | 1.50 | 1.60 |
| E2 | 2.17 | 2.27 | 2.37 |
| e | | 0.50 BSC | |
| L | 0.30 | 0.40 | 0.50 |
| L1 | 0.15 | 0.20 | 0.25 |
| L2 | 0.15 | 0.21 | 0.26 |
| L3 | 0.63 | 0.73 | 0.83 |
| L4 | 0.44 | 0.54 | 0.64 |
| L5 | 0.30 | 0.40 | 0.50 |
| L6 | 0.27 | 0.37 | 0.47 |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.08 | |

**NOTES:**

1. Dimensions are in millimeters.
2. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.
3. Dimension b applies to metallized terminal and is measured between 0.20mm and 0.35mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
4. Coplanarity applies to the terminals and all other bottom surface metallization.




**RECOMMENDED LAND PATTERN**

**NOTE:**

1. **Dimensions are in millimeters.**